FORM PTO-1390 (REV 12-29-99)

U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 843.39887X00 filed 03/19/01

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): 09/787380

INTERNATIONAL APPLICATION NO.: PCT/JP99/05012

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TITLE OF INVENTION: PLL CIRCUIT AND RADIO COMMUNICATION TERMINAL APPARATUS USING THE SAME

APPLICANT(S) FOR DO/EO/US: YAMAWAKI, TAIZO; ENDO, TAKEFUMI; WATANABE, KAZUO; HORI KAZUAKI and HILDERSLEY, JULIAN

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. [X] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [X] has been transmitted by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. [ ] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [ ] have been transmitted by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [X] A FIRST preliminary amendment.
    [ ] A SECOND or SUBSEQUENT preliminary amendment.
14. [ ] A substitute specification.
15. [X] A change of power of attorney and/or address letter.
16. [X] Other items or information:

International Preliminary Examination Report
PCT Request Form
International Publication No. WO00/18014
International Search Report
International Preliminary Examination Report
Figs. 1-9
Credit Card Payment Form

APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/787380	PCT/JP99/05012	843.39887X00

17. [X] The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

	CALCULATIONS PTO USE ONLY
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$970.00**	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$840.00**	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$690.00**	
International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$670.00**	
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) **$96.00**	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00
Surcharge of **$130.00** for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	20 - 20 =	0	X **$18.00**	$ 0.00
Independent claims	2 - 3 =	0	X **$78.00**	$ 0.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$260.00**	$ 0.00

TOTAL OF ABOVE CALCULATIONS =	$
Reduction of 1/2 for filing by small entity, if applicable. A Small Entity Statement must also by filed (Note 37 CFR 1.9, 1.27, 1.28).	$ 0.00
SUBTOTAL =	$ 860.00
Processing fee of **$130.00** for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +	$ 0.00
TOTAL NATIONAL FEE =	$ 860.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +	$ 0.00
TOTAL FEES ENCLOSED =	$
	Amount to be refunded: $
	charged: $

a. [X] A check in the amount of $860.00 to cover the above fees is enclosed.

b. [ ] Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 01-2135. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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SIGNATURE.

Gregory E. Montone
NAME

28,141
REGISTRATION NUMBER

843.39887X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: YAMAWAKI et al.

Serial No.: Not yet assigned

Filed: On even date

For: PLL CIRCUIT AND RADIO COMMUNICATION TERMINAL APPARATUS USING THE SAME

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

March 19, 2001

Sir:

Prior to examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel claims 10-14 without prejudice or disclaimer.

Please add the following new claims:

-- 15. The PLL circuit according to claim 2, wherein:

the variable-gain phase comparator comprises a Gilbert multiplier; first, second, third and fourth current mirror circuits; and a variable current source capable of varying an output constant current value, and

the PLL circuit inputs an output current of the variable current source to the first current mirror circuit; uses an output current of the first current mirror circuit as a bias current of the Gilbert multiplier; differentially inputs the first and second input signals to the Gilbert multiplier; inputs third and fourth signals, which are differential output current of the Gilbert multiplier, to the second and third current mirror circuits respectively; inputs an output current of the second current mirror circuit to the fourth current mirror circuit; and adds an output current of the third current mirror circuit and an output current of the fourth current mirror circuit so as to generate an output signal of the variable-gain phase comparator.

16. The PLL circuit according to claim 3, wherein:

the variable-gain phase comparator comprises a Gilbert multiplier; first, second, third and fourth current mirror circuits; and a variable current source capable of varying an output constant current value, and

the PLL circuit inputs an output current of the variable current source to the first current mirror circuit; uses an output current of the first current mirror circuit as a bias current of the Gilbert multiplier; differentially inputs the first and second input signals to the Gilbert multiplier; inputs third and fourth signals, which are differential output current of

the Gilbert multiplier, to the second and third current mirror circuits respectively; inputs an output current of the second current mirror circuit to the fourth current mirror circuit; and adds an output current of the third current mirror circuit and an output current of the fourth current mirror circuit so as to generate an output signal of the variable-gain phase comparator.

17. The PLL circuit according to claim 8, wherein:

the variable-gain phase comparator comprises a Gilbert multiplier; first, second, third and fourth current mirror circuits; and a variable current source capable of varying an output constant current value, and

the PLL circuit inputs an output current of the variable current source to the first current mirror circuit; uses an output current of the first current mirror circuit as a bias current of the Gilbert multiplier; differentially inputs the first and second input signals to the Gilbert multiplier; inputs third and fourth signals, which are differential output current of the Gilbert multiplier, to the second and third current mirror circuits respectively; inputs an output current of the second current mirror circuit to the fourth current mirror circuit; and adds an output current of the third current mirror circuit and an output current of the fourth current mirror circuit so as to generate an output signal of the variable-gain phase comparator.

18. The PLL circuit according to claim 9, wherein:

the variable-gain phase comparator comprises a Gilbert multiplier; first, second, third and fourth current mirror circuits; and a variable current source capable of varying an output constant current value, and

the PLL circuit inputs an output current of the variable current source to the first current mirror circuit; uses an output current of the first current mirror circuit as a bias current of the Gilbert multiplier; differentially inputs the first and second input signals to the Gilbert multiplier; inputs third and fourth signals, which are differential output current of the Gilbert multiplier, to the second and third current mirror circuits respectively; inputs an output current of the second current mirror circuit to the fourth current mirror circuit; and adds an output current of the third current mirror circuit and an output current of the fourth current mirror circuit so as to generate an output signal of the variable-gain phase comparator.

19. The PLL circuit according to claim 15, wherein:

the variable current source comprises a plurality of current mirror circuits, a plurality of switches, a control circuit and a reference current generating circuit;

by the control circuit, a base of each output transistor of the plurality of current mirror circuits is connected to an emitter of the output transistor or to a base of the input transistor of the current mirror circuit including the output

transistor, and

the PLL circuit inputs an output constant current of the reference current generating circuit to the plurality of current mirror circuits, and adds the output currents of the plurality of current mirror circuits so as to generate an output current of the variable current source.

20. The PLL circuit according to claim 16, wherein:

the variable current source comprises a plurality of current mirror circuits, a plurality of switches, a control circuit and a reference current generating circuit;

by the control circuit, a base of each output transistor of the plurality of current mirror circuits is connected to an emitter of the output transistor or to a base of the input transistor of the current mirror circuit including the output transistor, and

the PLL circuit inputs an output constant current of the reference current generating circuit to the plurality of current mirror circuits, and adds the output currents of the plurality of current mirror circuits so as to generate an output current of the variable current source.

21. The PLL circuit according to claim 17, wherein:

the variable current source comprises a plurality of current mirror circuits, a plurality of switches, a control circuit and a reference current generating circuit;

by the control circuit, a base of each output transistor

of the plurality of current mirror circuits is connected to an emitter of the output transistor or to a base of the input transistor of the current mirror circuit including the output transistor, and

the PLL circuit inputs an output constant current of the reference current generating circuit to the plurality of current mirror circuits, and adds the output currents of the plurality of current mirror circuits so as to generate an output current of the variable current source.

22. The PLL circuit according to claim 18, wherein:

the variable current source comprises a plurality of current mirror circuits, a plurality of switches, a control circuit and a reference current generating circuit;

by the control circuit, a base of each output transistor of the plurality of current mirror circuits is connected to an emitter of the output transistor or to a base of the input transistor of the current mirror circuit including the output transistor, and

the PLL circuit inputs an output constant current of the reference current generating circuit to the plurality of current mirror circuits, and adds the output currents of the plurality of current mirror circuits so as to generate an output current of the variable current source.

23. The PLL circuit according claim 5, wherein:

the phase comparator is replaced with a phase comparator

which is constructed in a manner that the variable current source of the variable-gain phase comparator described in claim 10 is replaced with a reference current generating circuit for generating a constant current output, and

an output signal amplitude from the variable-gain phase comparator inputted to the phase comparator is set smaller than $k \cdot T/q$.

24. The PLL circuit according claim 6, wherein:

the phase comparator is replaced with a phase comparator which is constructed in a manner that the variable current source of the variable-gain phase comparator described in claim 10 is replaced with a reference current generating circuit for generating a constant current output, and

an output signal amplitude from the variable-gain phase comparator inputted to the phase comparator is set smaller than $k \cdot T/q$.

25. A radio communication terminal apparatus, comprising:

a transmitter system including a quadrature modulator, to which I and Q signals are inputted, a PLL circuit connected to an output terminal of the quadrature modulator, and a power amplifier connected to an output terminal of the PLL circuit;

a receiver system outputting I and Q signals;

an antenna; and

an antenna switch interconnecting the antenna, the transmitter system and the receiver system,

the PLL circuit comprising the PLL circuit described in any of claims 1 to 19. --

REMARKS

Entry of this amendment prior to examination is respectfully requested.

Attached hereto is a marked version of the changes made to the claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (843.39887X00), and please credit any excess fees to said deposit account.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 10-14 have been cancelled.

Claims 15 to 25 have been added.

8/PTRS

SPECIFICATION

PLL CIRCUIT AND RADIO COMMUNICATION TERMINAL APPARATUS USING THE SAME

TECHNICAL FIELD

The present invention relates to a technique effectively applicable to a PLL circuit, which converts an IF (intermediate frequency) signal into an RF (radio frequency) signal in a plurality of operation frequency bands, and to a radio communication terminal apparatus using the PLL circuit.

BACKGROUND ART

The present inventors have made the following search and study. More specifically, currently, a great many of radio communication systems exist in the world. For this reason, a terminal usable a plurality of systems has been required. To give an example, there are a GSM (Global System for Mobile communications) and a DCS 1800 (Digital Cellular system 1800). These systems have similar modulation system although an operation frequency band is different.

A PLL circuit has been described in "Phase lock Techniques" (ISBN 0-471-04294-3) section 10.3 published by John Wiley & Sons Company. The PLL circuit converts an IF signal into an RF signal in one operation frequency band. Although the technique shown in Fig. 9 is not known, it shows one example in which the PLL circuit studied by the present inventors is

constructed so as to be usable in a plurality of operation frequency bands.

The above PLL circuit comprises a phase comparator 41, a mixer 2, n (n is two or more natural number) low-pass filters (LPF) 42-1 to 42-n, n voltage control oscillators (VCO) 4-1 to 4-n, n couplers 43-1 to 43-n, and a control circuit 6 for controlling the on/off of these VCOs 4-1 to 4-n.

Two signals are inputted to the phase comparator 41. A first input signal is a reference signal IF, and a second input signal is an output signal from the mixer 2. The reference IF signal and the output signal from the mixer 2 is compared in its phase, and then, a signal is outputted in proportional to a phase difference. An output signal from the phase comparator 41 is outputted to the LPFs 42-1 to 42-n so that unnecessary noise is eliminated, and thereafter, is inputted to the VCOs 4-1 to 4-n. The control circuit 6 operates one VCO of the above n VCOs in accordance with a desired operation frequency band, and then, other VCOs are controlled to an off state so as not to output a signal. The output frequencies of the VCOs 4-1 to 4-n are individually fVCO1 to fVCOn, and are inputted to the couplers 43-1 to 43-n. In the coupler, the input signal is outputted after being branched into two. A first output of the coupler is an output signal of the PLL circuit, and a second output thereof is inputted to the mixer 2. Two signals are inputted to the mixer 2, and a first input signal of the mixer is the second output signal of the couplers 43-1 to 43-n. A local oscillator signal RF-LO having a frequency fLO is inputted

to the second input of the mixer 2. An output frequency of the mixer 2 is an absolute value of difference between two input frequencies, that is, |fLO − fVCOn|. The output signal of the mixer 2 is the second input signal of the phase comparator 41. Now, if the VCO 4-n is operated, in a state that the PLL circuit is locked, two input frequencies of the phase comparator 41 become equal; for this reason, the input frequency is fIF = |fLO − fVCOn|. Therefore, an output frequency fVCOn of the VCO 4-n is obtained from |fLO − fIF|. Namely, the reference signal frequency fIF to the PLL circuit is converted into fVCOn = |fLO − fIF|.

An operation of the PLL circuit will be analyzed below using a linear model. In this case, the VCO 4-n is selected as the VCO. A phase difference conversion gain of the phase comparator 41 is set as Kd, and a sensitivity of the selected VCO 4-n is set as Kv. Moreover, a lag lead filter is used as the LPF 42-n. Thus, a transfer function F(s) of the LPF 42-n is obtained from the following equation (1).

$$F(s)=\frac{1+s\cdot C\cdot R2}{1+s\cdot C\cdot(R1+R2)} \tag{1}$$

Moreover, an open loop transfer function Ho of the PLL circuit is obtained from the following equation (2).

$$Ho=Kd\cdot Kv\cdot F(s) \tag{2}$$

The pole ωp and zero ωz of the above open loop transfer function Ho are obtained from the following equations (3) and (4), respectively.

$$\omega p = \frac{1}{C \cdot (R1 + R2)} \tag{3}$$

$$\omega z = \frac{1}{C \cdot R2} \tag{4}$$

When the above ωp and ωz are both smaller than a loop band K of the PLL circuit, the loop band K is obtained from the following equation (5).

$$K = Kd \cdot Kv \cdot \frac{R2}{R1 + R2} \tag{5}$$

Therefore, the above loop band K is determined by the aforesaid Kd, Kv, and the transfer function F(s) of the LPF 42-n. The above Kd is a constant; however, in general, the above Kv is different depending upon an operation frequency band. Thus, the characteristics of the LPFs 42-1 to 42-n must be designed in accordance with the above Kv.

By the way, the present inventors have made the study of the aforesaid PLL circuit; as a result, they have found the following matter. More specifically, the aforesaid PLL circuit requires n LPFs for using the plurality of operation frequency bands. In general, the phase comparator is built in

an IC; on the other hand, the LPF is mounted outside the IC. For this reason, the number of components mounted outside increases; as a result, a problem arises such that terminal mounting becomes complicate, and the mounting area increases. Further, in the case of using n LPFs, the IC requires n pins corresponding to n LPFs; for this reason, a problem arises such that the number of pins increases. Furthermore, a design must be made with respect to each of n LPFs; for this reason, a problem arises such that the design of LPF becomes complicate.

It is, therefore, an object of the present invention to provide a PLL circuit, which reduces the number of n LPFs required in the above PLL circuit to only one LPF, and thereby, can reduce a mounting area and the number of pins, and can simplify a design, and to provide a radio communication terminal apparatus using the PLL circuit.

The above, other objects and novel features of the present invention will be more apparently understood from the description of this specification and the accompanying drawings.

DISCLOSURE OF THE INVENTION

The following is a brief description on the summary of principal constituent features of the invention disclosed in this application.

More specifically, in order to achieve the above object, the present invention provides a PLL circuit, characterized by comprising: a variable-gain phase comparator outputting a

signal proportional to a phase difference between a first input signal and a second input signal, and varying a phase difference gain; a low-pass filter connected to an output terminal of the variable-gain phase comparator; n VCOs connected to an output terminal of the low-pass filter; n couplers connected one by one to an output terminal of the VCOs; a frequency converter connected to each output terminal of n couplers, and converting a frequency of addition signal of the output signal from n couplers so as to output the second input signal; and a control circuit controlling an on-off of operation of n VCOs.

Further, in order to achieve the above object, the PLL circuit is constructed in a manner that the variable-gain phase comparator is replaced with a phase comparator in which a phase difference conversion gain changes by the second signal amplitude, and a variable gain amplifier capable of varying a gain is interposed between the phase comparator and the frequency converter.

Further, in order to reduce an output noise of the PLL circuit, the PLL circuit is constructed in a manner m pieces ("m" is a natural number) of LPFs connected in parallel are connected between the frequency converter and the variable-gain phase comparator, or to the first input of the variable-gain phase comparator, and the PLL circuit further includes a control circuit for controlling an on-off of operation of these m pieces of LPFs connected in parallel.

Moreover, the present invention provides a radio communication terminal apparatus, characterized by

comprising: a transmitter system including a quadrature modulator, to which I and Q signals are inputted, a PLL circuit connected to an output terminal of the quadrature modulator, and a power amplifier connected to an output terminal of the PLL circuit; a receiver system outputting I and Q signals; an antenna; and an antenna switch interconnecting the antenna, the transmitter system and the receiver system, the PLL circuit comprising the PLL circuit described above.

The following is a description on the effects obtained by the principal constituent feature of the invention disclosed in this application.

According to the present invention, in the PLL circuit converting an IF signal into an RF signal, it is possible to reduce the number of LPFs required in the case of being used in a plurality of operation frequency bands to only one. Therefore, it is possible to reduce a mounting area and the number of pins of IC including the phase comparator, and thus, to simplify a design of the PLL circuit. As a result, it is possible to reduce the mounting area of a radio communication terminal apparatus such as a cellular phone using the PLL circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a view showing a configuration of PLL circuit according to a first embodiment of the present invention;

Fig. 2 is a view showing a configuration of variable-gain phase comparator and a variable current source used in the

PLL circuit according to the first embodiment of the present invention;

Fig. 3 is a view showing a configuration of variable current source used in the PLL circuit according to the first embodiment of the present invention;

Fig. 4 is a view showing a configuration of PLL circuit according to a second embodiment of the present invention;

Fig. 5 is a view showing a phase comparator, which can vary a gain by input amplitude in the PLL circuit according to a second embodiment of the present invention;

Fig. 6 is a view showing a configuration of PLL circuit according to a third embodiment of the present invention;

Fig. 7 is a view showing a configuration of radio communication terminal apparatus using the PLL circuit of the present invention;

Fig. 8 is a view showing a configuration of cellular phone used as the radio communication terminal apparatus using the PLL circuit of the present invention; and

Fig. 9 is a view showing a configuration of conventional PLL circuit recited as the premise of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

The embodiments of the present invention will be described below with reference to the accompanying drawings. In all figures for explaining the embodiments, like reference numerals are used to designate the same components, and the repeated explanation is omitted.

(Embodiment 1)

Fig. 1 is a view showing a configuration of PLL circuit according to a first embodiment of the present invention.

The PLL circuit of the present invention comprises a variable-gain phase comparator 1, a mixer 2, an LPF 3, n pieces of VCOs 4-1 to 4n, n pieces of couplers 5-1 to 5-n, and a control circuit 6 for controlling the on/off of the operation of the VCOs.

Two signals are inputted to the variable-gain phase comparator 1. A first input signal is a reference signal IF having a frequency of fIF, and a second input signal is an output signal from the mixer 2. The variable-gain phase comparator 1 compares the reference signal IF with the output signal from the mixer 2 so as to output a signal proportional to a phase difference between these signals. Then, the output signal from the variable-gain phase comparator 1 is inputted to the VCOs 4-1 to 4n after an unnecessary noise is eliminated by the LPF 3. Each output signal of the VCOs 4-1 to 4-n is inputted to one of the couplers 5-1 to 5-n. By the control circuit 6, one of the VCOs 4-1 to 4-n is operated in accordance with a desired operation frequency band; on the other hand, other VCOs are controlled to an off state so as not to output a signal. Each of the couplers 5-1 to 5-n branches the input signal, and then, outputs a signal from two ports. A first output signal of these couplers 5-1 to 5-n is an output signal of the PLL circuit, and a second output signal thereof is inputted to the mixer 2. Two signals are inputted to the mixer 2, and a first input signal

of the mixer 2 is the second output signal of the couplers 5-1 to 5-n. A local oscillator signal RF-LO having a frequency fLO is inputted to a second input of the mixer 2. Now, if the VCO 4-n is operated, an output frequency of the mixer 2 is an absolute value of a difference in frequency between the first and second input signals, that is, $|fLO - fVCOn|$. Thus, the output signal of the mixer 2 becomes a second input signal of the variable-gain phase comparator 1. In a state that the PLL circuit is locked, two input frequencies of the variable-gain phase comparator 1 becomes equal, that is, $fIF = |fLO - fVCOn|$. Therefore, the output frequency fVCOn of the VCO 4-n is obtained from $|fLO - fIF|$. In other words, the reference frequency fIF to the PLL circuit is converted into $fVCOn = |fLO - fIF|$.

The analysis of the operation of the PLL circuit has been made using a linear model in the same manner as the case of the above-mentioned PLL circuit shown in Fig. 9. In the above equation (5), one LPF 3 is used in the PLL circuit; for this reason, R1 and R2 are a constant. The aforesaid loop band K is determined by the product of the phase difference conversion gain Kd and the sensitivity Kv of the VCO 4-n. Therefore, in accordance with the sensitivity of the VCOs 4-1 to 4-n, the above loop band Kd is varied, and thereby, the optimization of the loop band K can be performed by only one LPF.

Fig. 2 shows a configuration of the variable-gain phase comparator 1.

The variable-gain phase comparator 1 comprises 14 transistors Q1 to Q14, and a variable current source 7

generating a variable output current IREF. A bipolar transistor is used as these transistors Q1 to Q14. A reference numeral 8 denotes a Gilbert multiplier, and the details are described in "Analog integrated circuit design technology for Ultra SLI (the last volume)", section 10.3 published by Baifukan Company. Differential signals VREF+ and VREF- are inputted to a first input of the Gilbert multiplier 8; on the other hand, differential signals VIF+ and VIF- are inputted to a second input of the same. In the Gilbert multiplier 8, the two differential signals are multiplied so that differential currents I1 and I2 are outputted. The amplitude of two input signals of the Gilbert multiplier 8 is large. Thus, in the case where the transistors Q1 to Q6 make a switching operation, when a collector current of the transistor Q8 is set as I3, a phase difference Φ between the above two input signals and an output differential current (I2 − I1) of the Gilbert multiplier 8 are obtained from the following equation (6).

$$I2 - I1 = I3 \cdot (\frac{2 \cdot \phi}{\pi} - 1) \tag{6}$$

The transistors Q7 and Q8 constitute a current mirror circuit, and when a current mirror ratio is set as "a", the following relation of I3 = a · IREF is formed. Further, the transistors Q9 and Q10 constitute a current mirror circuit, and when a current mirror ratio is set as "b", the following relation of I4 = b · I1 is formed. Further, the transistors Q11 and Q12

constitute a current mirror circuit, and when a current mirror ratio is set as "b", the following relation of I5 = b · I2 is formed. Further, the transistors Q13 and Q14 constitute a current mirror circuit, and when a current mirror ratio is set as "1", the following relation of I6 = I4 is formed. Thus, an output current (I5 - I6) of the variable-gain phase comparator 1 is obtained from the following equation (7).

$$I5 - I6 = a \cdot b \cdot IREF \cdot (\frac{2 \cdot \phi}{\pi} - 1) \quad (7)$$

Therefore, the phase difference conversion gain Kd of the variable-gain phase comparator 1 is obtained from the following equation (8).

$$Kd = \frac{2 \cdot a \cdot b \cdot IREF}{\pi} \quad (8)$$

In the above equation, "a" and "b" are a constant, and thus, the phase difference conversion gain Kd is proportional to IREF. Therefore, the phase difference conversion gain Kd is variable by varying IREF.

Fig. 3 is a view showing a circuit configuration of the variable current source 7 which can supply two kinds of constant currents having a current value of 1:2.

The variable current source 7 comprises transistors Q15 to Q18, a reference current generating circuit 9 for outputting a constant current, switches S1 and S2, and a control circuit

10 for controlling these switches S1 and S2. The transistors Q15 to Q18 have the same size, and a bipolar transistor is used as these transistors Q15 to Q18. By the switch S1, a base of the transistor Q16 is connected with an emitter of the transistor Q16 or a base of the transistor Q15. Moreover, by the switch S2, a base of the transistor Q17 is connected with an emitter of the transistor Q17 or the base of the transistor Q15, and a base of the transistor Q18 is connected with an emitter of the transistor Q18 or the base of the transistor Q15. These transistors Q16 to Q18 constitute a current mirror circuit together with the transistor Q15. The transistor Q15 is called as an input transistor of the current mirror circuit because a current is inputted thereto from the reference current generating circuit 9; on the other hand, the transistors Q 16 to Q18 are called as an output transistor because they outputs a current from their collectors. When a current supplied from the reference current generating circuit 9 is set as I7, each collect current of the transistors Q16 to Q18 is I7 because these transistors Q15 to Q18 have the same size. In the case where the base of the transistor Q16 is connected to the base of the transistor Q15 and the bases of the transistors Q17 and Q18 are individually connected to the emitters of transistors Q17 and 18, no collector current flows to the transistors Q17 and Q18 because a voltage between base and emitter is 0V. Therefore, the IREF is equal to the collector current of the transistor Q16; namely becomes I7. Moreover, in the case where the base of the transistor Q16 is connected to the emitter of the

a phase comparator 11 varying a gain by input amplitude is used in place of the variable-gain phase comparator 1 used in the first embodiment, and further, a variable gain amplifier 12 is interposed between the mixer 2 and the phase comparator 11. The gain of the variable gain amplifier 12 is controlled in accordance with the sensitivity of the VCOs 4-1 to 4-n, and the input amplitude to the phase comparator 11 is varied so as to change a gain of the phase comparator 11, and thereby, a loop band of the PLL circuit can be optimized.

Fig. 5 is a view showing a configuration of the phase comparator 11.

The phase comparator 11 used in the second embodiment is a circuit having the following features that a reference current generating circuit 13 for outputting a constant current IREF is used in place of the variable constant source 7 of Fig. 2. A bipolar transistor is used as the transistors Q1 to Q14.

The details of operation of the above phase comparator 11 have been described, for example, in the document, A. Bilotti, "Applications of a Monolithic Analog Multiplier," IEEE J. Solid-State Circuits, vol. SC-3, pp. 373-380, Dec. 1968. According to the above document, there are cited the following two ways to change a gain of the phase comparator 11 by input amplitude.

1. The amplitude of inputs 1 and 2 is set smaller than $k \cdot T/q$ so that the transistors Q1 to Q6 make no switching operation.

2. One of the inputs 1 and 2 has amplitude larger than

k·T/q so that the transistors Q1 to Q6 make a switching operation, and the other thereof has amplitude smaller than k · T/q so that the transistors Q1 to Q6 make no switching operation. In this case, k is a Boltzmann constant, T is an absolute temperature, and q is a charge of electron.

Therefore, according to this second embodiment, the gain of the variable gain amplifier 12 is controlled in accordance with the sensitivity of the VCOs 4-1 to 4-n so as to change the gain of the phase comparator 11. By doing so, like the above first embodiment, the number of LPF 3 required for the PLL circuit can be reduced to only one. Therefore, it is possible to reduce the number of pins of IC in which the phase comparator 11 is built, and thus, to simplify a design of the PLL circuit.

(Embodiment 3)

Next, the following is a description on a PLL circuit according to a third embodiment of the present invention.

Fig. 6 is a view showing a configuration of the PLL circuit according to the third embodiment of the present invention.

The PLL circuit of this third embodiment is a circuit having the following features. More specifically, LPFs 16-1 to 16-m connected in parallel are interposed between the variable-gain phase comparator 1 and the mixer 2 used in the above first embodiment, and LPFs 15-1 to 15-m connected in parallel are connected to the first input of the variable-gain phase comparator 1. Further, a control circuit 14 for controlling the on-off of the VCOs 4-1 to 4-n, LPFs 15-1 to 15-m, and LPFs 16-1 to 16-m is used in place of the control circuit

6.

These LPFs 15-1 to 15-m and LPFs 16-1 to 16-m are used for eliminating a noise inputted to the variable-gain phase comparator 1. Moreover, the reference signal IF has m-way frequencies fIF. The control circuit 14 selects one LPF having the optimal cut-off frequency to fIF from the respective LPFs 15-1 to 15-m. Likewise, the control circuit 14 selects one LPF having the optimal cut-off frequency to fIF from the respective LPFs 16-1 to 16-m.

Next, the following is a description on a radio communication terminal apparatus using the PLL circuit according to the present invention.

Fig. 7 is a view showing a configuration of the radio communication terminal apparatus using the PLL circuit of the present invention.

The radio communication terminal apparatus of the present invention comprises a transmitter system including a quadrature modulator 17, the PLL circuit 18 and a power amplifier 19; an antenna switch 20; an antenna 21; and a receiver system 22.

In the quadrature modulator 17, the IF signal is modulated by I and Q signals. An output signal from the quadrature modulator 17 is inputted as a reference signal to the PLL circuit 18. The reference signal and a RF-LO signal are inputted to the PLL circuit, and then, one of frequencies fVCO1 to fVCOn is outputted as an output signal frequency. The output signal of the PLL circuit 18 is amplified in its power by the power amplifier 19, and thereafter, is transmitted from the antenna

21 via the antenna switch 20. In transmitting, only antenna 21 and transmitter system 23 are connected by the antenna switch 20; on the other hand, in receiving, only antenna 21 and receiver system 22 are connected. A signal received by the antenna 21 is inputted to the receiver system 22 via the antenna switch 20, and then, is demodulated so that the signals I and Q are outputted.

Next, a detailed example of the radio communication terminal apparatus of the present invention will be described below.

Fig. 8 is a view showing a configuration of cellular phone used as the radio communication terminal apparatus of the present invention.

The cellular phone of the present invention has a circuit configuration in the case of using two frequency bands (communication methods). The cellular phone comprises a microphone 24, a transmitter side A-D converter 25, a digital signal processing unit 26 used in common to reception and transmission, a transmitter side D-A converter 27, the transmitter system 23, the antenna switch 20, the receiver system 22, a receiver side A-D converter 28, a receiver side D-A converter 29, and a speaker 30.

The transmitter system 23 is provided with two power amplifiers 19-1 and 19-2 corresponding to two frequency bands. The frequency fVCO1 and fVCO2 signals outputted from the PLL circuit 18 are amplified in its power by the power amplifiers 19-1 and 19-2, respectively, and thereafter, are outputted.

These power amplifiers 19-1 and 19-2 have the same function as the power amplifier 19 described before. Moreover, a local oscillation signal 1 (IF) is inputted to a quadrature modulator 17, and a local oscillator signal 2 (RF-LO) is inputted to the PLL circuit 18, and these modulator and PLL circuit have the same function as described above.

The receiver system 22 is provided with two band-pass filters 31-1 and 32-2, LANs 32-1 and 32-2, pass-band filters 33-1 and 33-2, mixers 34-1 and 34-2; a common pass-band filter 35 after mixing; a mixer 36; a pass-band filter 37; a variable gain amplifier 38, and a quadrature demodulator 39. More specifically, local oscillator signals 3a and 3b are inputted to mixers 34-1 and 34-2, respectively, and a local oscillator signal 4 is inputted to the mixer 36, and further, a local oscillator signal 5 is inputted to the quadrature demodulator 39.

In the receiver system 22, each of the mixers 34-1, 34-2 and 36 outputs the result multiplying two input signals, and thereby, frequency conversion can be performed. The local oscillator signal inputted to each of these mixers 34-1, 34-2 and 36 is a signal having a stable frequency outputted from a PLL synthesizer. The PLL synthesizer uses an output signal of crystal oscillator as a reference signal, and thereby, the output frequency can be stabilized. The band-pass filters 31-1, 31-2, 33-1, 33-2, 35 and 37 are a filter for passing only specified frequency band. In general, a dielectric filter is used as the band-pas filters 31-1 and 31-2, and a SAW filter

is used as the band-pass filters 33-1, 33-2 and 35, and further, an LC filter is used as the band-pass filter 37. The variable gain amplifier 38 is an amplifier for changing a gain by a control signal from the digital signal processing unit 26, and there are an analog type amplifier and a digital type amplifier. Each of the LANs 32-1 and 32-2 is an amplifier, which has almost no noise, and comprises one transistor and a bias circuit, in general.

In the above cellular phone, in transmitting, a voice (speech) is inputted through the microphone 24, and then, an analog signal from the microphone 24 is converted into a digital signal by the A-D converter 25 so that the digital signal is processed by the digital signal processing unit 26. Further, the digital signal from the digital signal processing unit 26 is converted into an analog signal by the D-A converter 27, and thereafter, the analog signal is outputted to the transmitter system 23. Then, in the transmitter system, 23, the same operation as described before is made, and a signal amplified by one of the power amplifiers 19-1 and 19-2 is transmitted from the antenna 21 via the antenna switch 20.

Moreover, in receiving, a signal received by the antenna 21 is inputted to the receiver system 22 via the antenna switch 20. Thereafter, the signal is passed through the path of the band-pass filter 31-1, the LAN 32-1, the band-pass filter 33-1 and the mixer 34-1 or the path of the band-pass filter 31-2, the LAN 32-2, the band-pass filter 33-2 and the mixer 34-2. Further, filtering, amplification and mixing are repeated are

filtered by the band-pass filter 35, the mixer 36 and the band-pass filter 37, and then, the signal is demodulated by the variable gain amplifier 38 and the quadrature demodulator 39, and thereafter, the signals I and Q are outputted from the receiver system 22. Then, an analog signal from the receiver system 22 is used as input, and the analog signal is converted into a digital signal by the A-D converter 28. Further, the digital signal is processed by the digital signal processing unit 26, and then, the digital signal from the digital signal processing unit 26 is converted into an analog signal by the D-A converter 29, and thereafter, the analog signal is outputted as a voice via the speaker 30.

Therefore, according to this third embodiment, the variable-gain phase comparator 1 is used as the phase comparator of the PLL circuit, and thereby, one VCO is operated in accordance with a desired operation frequency band. Moreover, the phase difference conversion gain is changed in accordance with the sensitivity of the VCOs 4-1 to 4-n, and thereby, like the above first embodiment, the number of LPF 3 required for the PLL circuit can be reduced to only one. Therefore, it is possible to reduce the number of pins of IC in which the phase comparator is built, and thus, to simplify a design of the PLL circuit. In addition, it is possible to eliminate a noise inputted to the variable-gain phase comparator 1 by the LPFs 15-1 to 15-n and 16-1 to 16-n. In the case where the PLL circuit is applied to a radio communication terminal apparatus such as a cellular phone or the like, it is possible to reduce a mounting

area of the radio communication terminal apparatus.

The invention made by the inventors has been described based on the above embodiments. The present invention is not limited to the above embodiments, and various modifications and changes may be possible within a range of scope without diverging the gist of the invention.

For example, the above embodiment has described the case where the frequency converter of the PLL circuit comprises a mixer circuit having two inputs. The frequency converter may comprise a divider circuit in place of the mixer circuit. In this case, an addition signal of the output signal from the coupler is used as input, and then, an output of the addition signal is inputted to the variable-gain phase comparator.

Further, a bipolar transistor has been used as the transistor of the circuit element in Fig. 2, Fig. 3 and Fig. 5. Another kind of transistor, for example, a MOSFET transistor may be used; in this case, the same function as the bipolar transistor can be realized.

Furthermore, the cellular phone shown in Fig. 8 has a circuit configuration of the case of using two frequency bands. The power amplifier, band-pass filter, LAN, mixer are connected in parallel, and thereby, it is possible to provide a circuit configuration capable of using many frequency bands.

INDUSTRIAL APPLICABILITY

As is evident from the above description, the present invention provides a PLL circuit, which can convert an IF

(intermediate frequency) signal into an RF (radio frequency) in a plurality of operation frequency bands. In the PLL circuit, the number of LPF required for the PLL circuit is reduced to only one, and thereby, it is possible to reduce the mounting area and the number of pins, and thus, to simplify a design of the PLL circuit. Further, the present invention is widely applicable to a radio communication terminal apparatus including a cellular phone using the PLL circuit, etc.

CLAIMS

1. A PLL circuit, comprising:

a variable-gain phase comparator outputting a signal proportional to a phase difference between a first input signal and a second input signal, and varying a phase difference gain;

a low-pass filter connected to an output terminal of the variable-gain phase comparator;

a plurality of VCOs connected to an output terminal of the low-pass filter;

a plurality of couplers connected one by one to an output terminal of the plurality of VCOs;

a frequency converter connected to each output terminal of the plurality of couplers, and converting a frequency of addition signal of the output signal from the plurality of couplers so as to output the second input signal; and

a control circuit controlling an on-off of operation of the plurality of VCOs.

2. The PLL circuit according to claim 1, wherein:

the frequency converter comprises a mixer circuit having two inputs; the addition signal of the output signal from the plurality of couplers is inputted to one of the two inputs; a local oscillator signal is inputted to the other of the two inputs; and the frequency converter inputs an output of the mixer circuit to the variable-gain phase comparator.

3. The PLL circuit according to claim 1, wherein:

the frequency converter comprises a divider; the addition signal of the output signal from the plurality of couplers is inputted to the frequency converter; and the frequency converter inputs an output of the divider circuit to the variable-gain phase comparator.

4. The PLL circuit according to claim 1, wherein:

the variable-gain phase comparator is replaced with a phase comparator in which a phase difference conversion gain changes by the second signal amplitude, and a variable gain amplifier capable of varying a gain is interposed between the phase comparator and the frequency converter.

5. The PLL circuit according to claim 4, wherein:

the frequency converter comprises a mixer circuit having two inputs; the addition signal of the output signal from the plurality of couplers is inputted to one of the two inputs; a local oscillator signal is inputted to the other of the two inputs; and the frequency converter inputs an output of the mixer circuit to the phase comparator via the variable gain amplifier.

6. The PLL circuit according to claim 4, wherein:

the frequency converter comprises a divider; the addition signal of the output signal from the plurality of couplers is inputted to the frequency converter; and the frequency converter inputs an output of the divider circuit to the phase

comparator via the variable gain amplifier.

7. The PLL circuit according to claim 1, wherein:

a plurality of low-pass filters connected in parallel is connected between the frequency converter and the variable-gain phase comparator, or is connected to the first input of the variable-gain phase comparator, and the PLL circuit further includes a control circuit for controlling an on-off of operation of the low-pass filters connected in parallel.

8. The PLL circuit according to claim 7, wherein:

the frequency converter comprises a mixer circuit having two inputs; the addition signal of the output signal from the plurality of couplers is inputted to one of the two inputs; a local oscillator signal is inputted to the other of the two inputs; and the frequency converter inputs an output of the mixer circuit to the variable-gain phase comparator.

9. The PLL circuit according to claim 7,wherein:

the frequency converter comprises a divider; the addition signal of the output signal from the plurality of couplers is inputted to the frequency converter; and the frequency converter an output of the divider circuit to the variable-gain phase comparator.

10. The PLL circuit according to claims 2, 3, 8 or 9, wherein:

the variable-gain phase comparator comprises a Gilbert

multiplier; first, second, third and fourth current mirror circuits; and a variable current source capable of varying an output constant current value, and

the PLL circuit inputs an output current of the variable current source to the first current mirror circuit; uses an output current of the first current mirror circuit as a bias current of the Gilbert multiplier; differentially inputs the first and second input signals to the Gilbert multiplier; inputs third and fourth signals, which are differential output current of the Gilbert multiplier, to the second and third current mirror circuits respectively; inputs an output current of the second current mirror circuit to the fourth current mirror circuit; and adds an output current of the third current mirror circuit and an output current of the fourth current mirror circuit so as to generate an output signal of the variable-gain phase comparator.

11. The PLL circuit according to claim 10, wherein:

the variable current source comprises a plurality of current mirror circuits, a plurality of switches, a control circuit and a reference current generating circuit;

by the control circuit, a base of each output transistor of the plurality of current mirror circuits is connected to an emitter of the output transistor or to a base of the input transistor of the current mirror circuit including the output transistor, and

the PLL circuit inputs an output constant current of the

reference current generating circuit to the plurality of current mirror circuits, and adds the output currents of the plurality of current mirror circuits so as to generate an output current of the variable current source.

12. The PLL circuit according claim 5 or 6, wherein:

the phase comparator is replaced with a phase comparator which is constructed in a manner that the variable current source of the variable-gain phase comparator described in claim 10 is replaced with a reference current generating circuit for generating a constant current output, and

an output signal amplitude from the variable-gain phase comparator inputted to the phase comparator is set smaller than $k \cdot T/q$.

13. A radio communication terminal apparatus, comprising:

a transmitter system including a quadrature modulator, to which I and Q signals are inputted, a PLL circuit connected to an output terminal of the quadrature modulator, and a power amplifier connected to an output terminal of the PLL circuit;

a receiver system outputting I and Q signals;

an antenna; and

an antenna switch interconnecting the antenna, the transmitter system and the receiver system,

the PLL circuit comprising the PLL circuit described in any of claims 1 to 12.

14. The radio communication terminal apparatus according to claim 13, wherein:

the radio communication terminal apparatus comprises a cellular phone including:

a microphone for inputting a voice as an analog signal;

a first A-D converter for converting the analog signal from the microphone into a digital signal;

a first digital signal processing unit for processing the digital signal from the first A-D converter;

a first D-A converter for converting a digital signal from the first digital processing unit into an analog signal, and for outputting the analog signal to the transmitter system;

a second A-D converter for inputting thereto the analog signal from the receiver system so as to convert the analog signal into a digital signal;

a second digital signal processing unit for processing the digital signal from the second A-D converter;

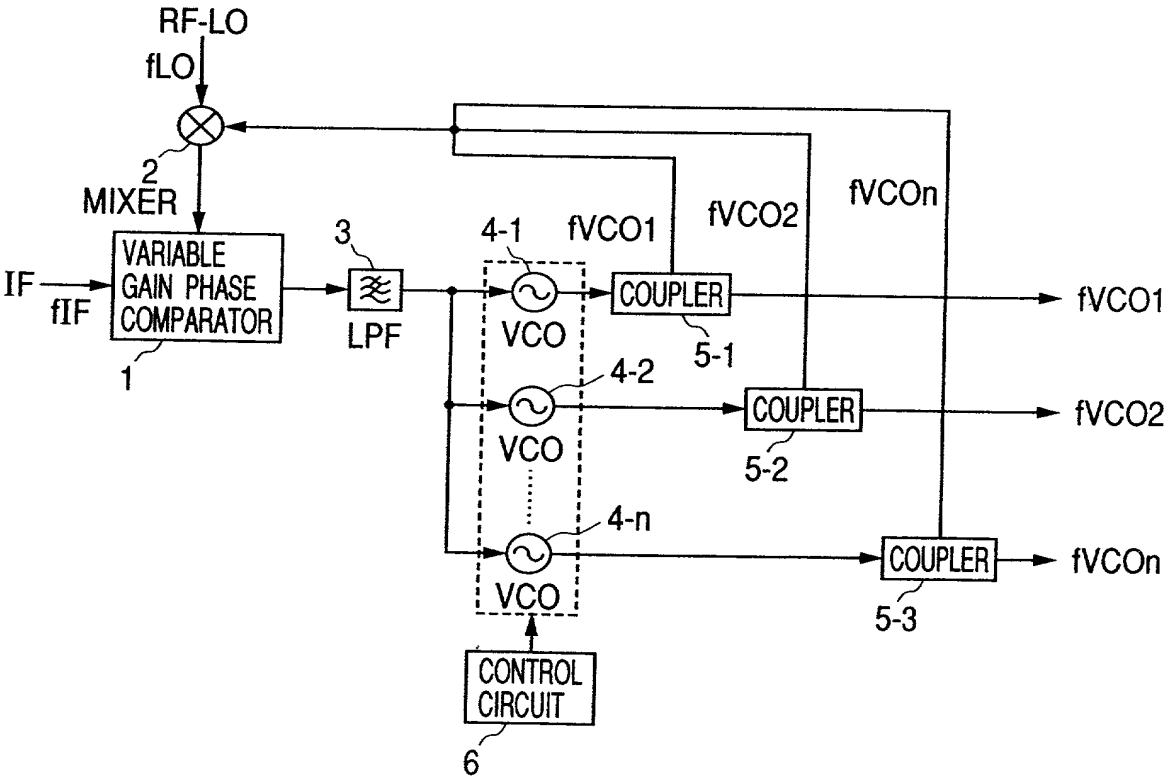
a second D-A converter for converting the digital signal from the second digital signal processing unit into an analog signal; and

a speaker for outputting the analog signal from the second D-A converter as a voice.

ABSTRACT

A PLL circuit and a radio communication terminal apparatus using the PLL circuit is provided. In the PLL circuit, the number of n pieces of LPFs which have been required is reduced to only one LPF, so that the PLL circuit can reduce a mounting area and the number of pins, and can simplify its design. The PLL circuit according to the present invention comprises a variable-gain phase comparator 1, a mixer 2, an LPF 3, n pieces of VCOs 4-1 to 4n, n pieces of couplers 5-1 to 5-n, and a control circuit 6 for controlling the on/off of the operation of the VCOs. The variable-gain phase comparator 1 is a phase comparator capable of varying a phase difference gain. By the control circuit 6, the on/off of the operation of the VCOs 4-1 to 4n and one of the VCOs 4-1 to 4-n is operated in accordance with a desired operation frequency band; other VCOs are controlled to an off state. The phase difference conversion gain is varied in accordance with the sensitivity of the VCOs 4-1 to 4-n, and thereby, the number of LPF required for the PLL circuit can be reduced to only one.

FIG. 1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COMPARATOR
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COUPLER
5-1
fVCO1
fVCO2
4-2
VCO
COUPLER
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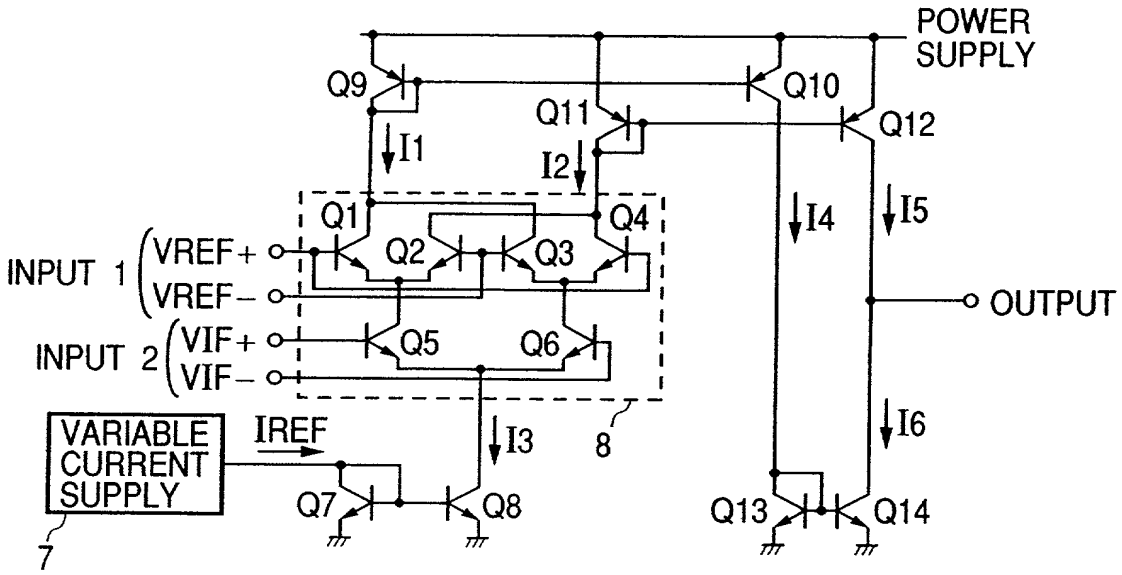
COUPLER
5-3
fVCOn
CONTROL
CIRCUIT
6

FIG. 2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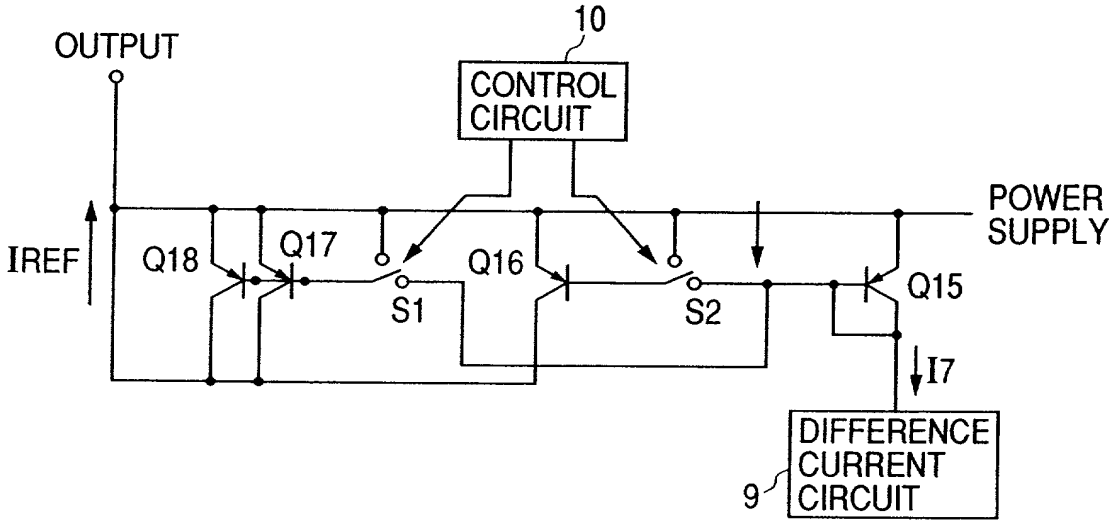
Q10
Q11
Q12
I1
I2
I4
I5
Q1
Q4
Q2
Q3
INPUT 1
VREF+
VREF−
INPUT 2
VIF+
VIF−
OUTPUT
Q5
Q6
I6
VARIABLE CURRENT SUPPLY
IREF
I3
8
7
Q7
Q8
Q13
Q14

FIG. 3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OUTPUT
CONTROL CIRCUIT
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Q18
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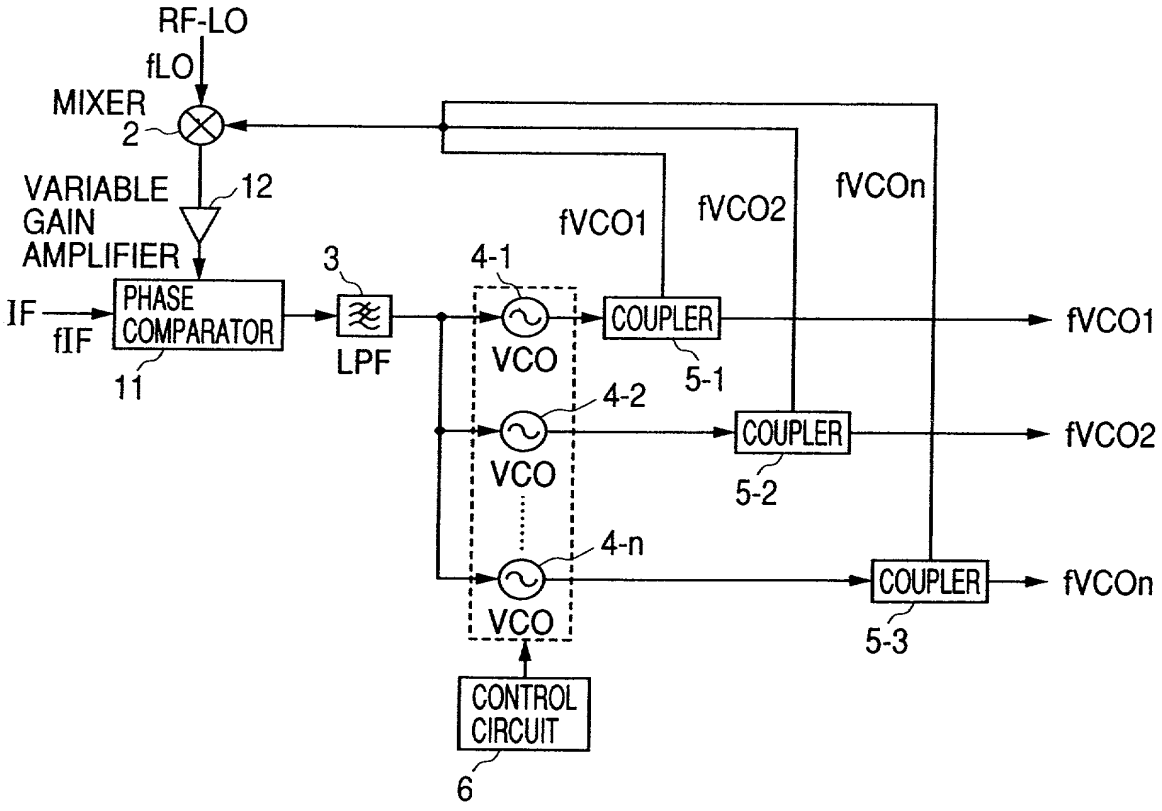
Q16
Q15
S1
S2
I7
DIFFERENCE CURRENT CIRCUIT
9

FIG. 4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GAIN
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12
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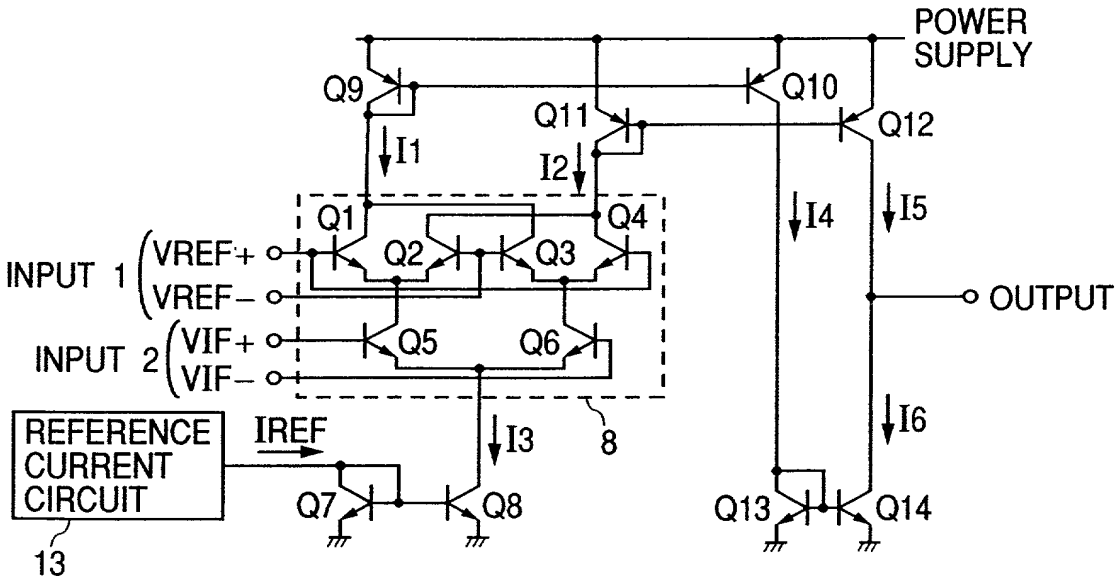
fIF
PHASE
COMPARATOR
11
3
LPF
4-1
VCO
4-2
VCO
4-n
VCO
fVCO1
fVCO2
fVCOn
COUPLER
5-1
COUPLER
5-2
COUPLER
5-3
fVCO1
fVCO2
fVCOn
CONTROL
CIRCUIT
6

FIG. 5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Q10
Q11
Q12
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I2
I4
I5
Q1
Q4
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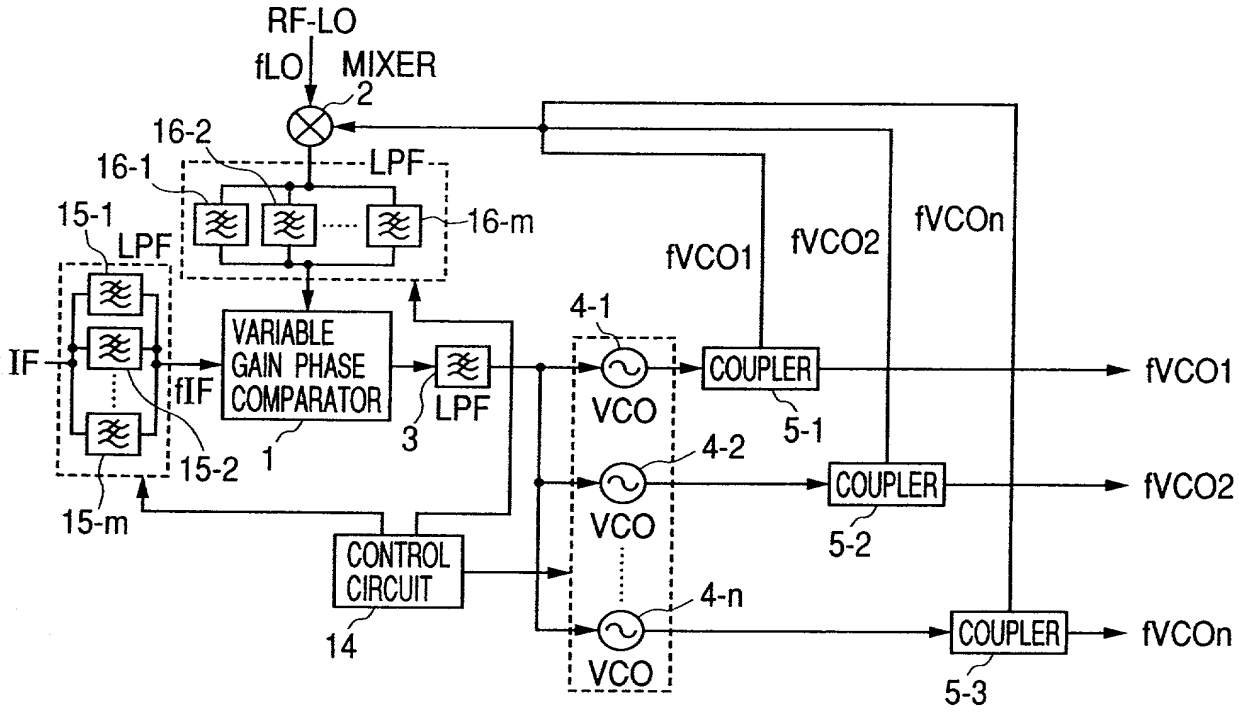
VREF−
Q2
Q3
OUTPUT
INPUT 2
VIF+
VIF−
Q5
Q6
I6
REFERENCE CURRENT CIRCUIT
IREF
I3
8
Q7
Q8
Q13
Q14
13

FIG. 6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16-2
16-1
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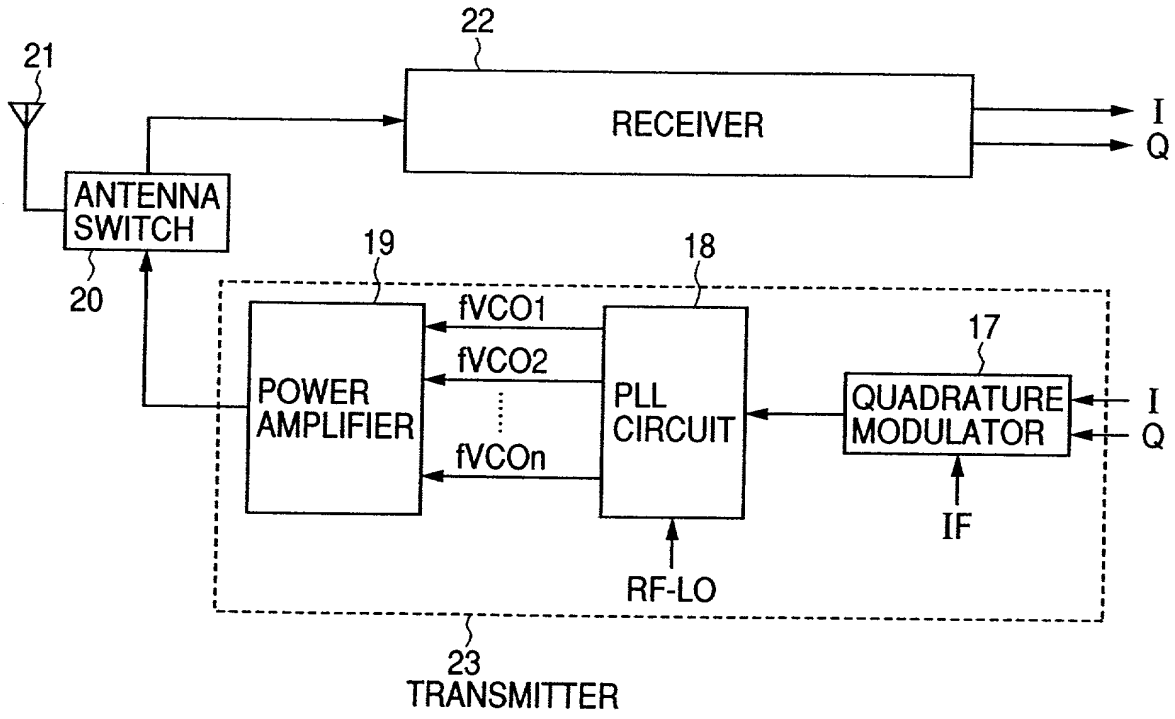
16-m
15-1
LPF
15-2
15-m
IF
fIF
VARIABLE GAIN PHASE COMPARATOR
1
3
LPF
CONTROL CIRCUIT
14
4-1
VCO
4-2
VCO
4-n
VCO
fVCO1
fVCO2
fVCOn
COUPLER
5-1
COUPLER
5-2
COUPLER
5-3
fVCO1
fVCO2
fVCOn

FIG. 7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21
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Q
ANTENNA SWITCH
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19
18
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fVCO2
fVCOn
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PLL CIRCUIT
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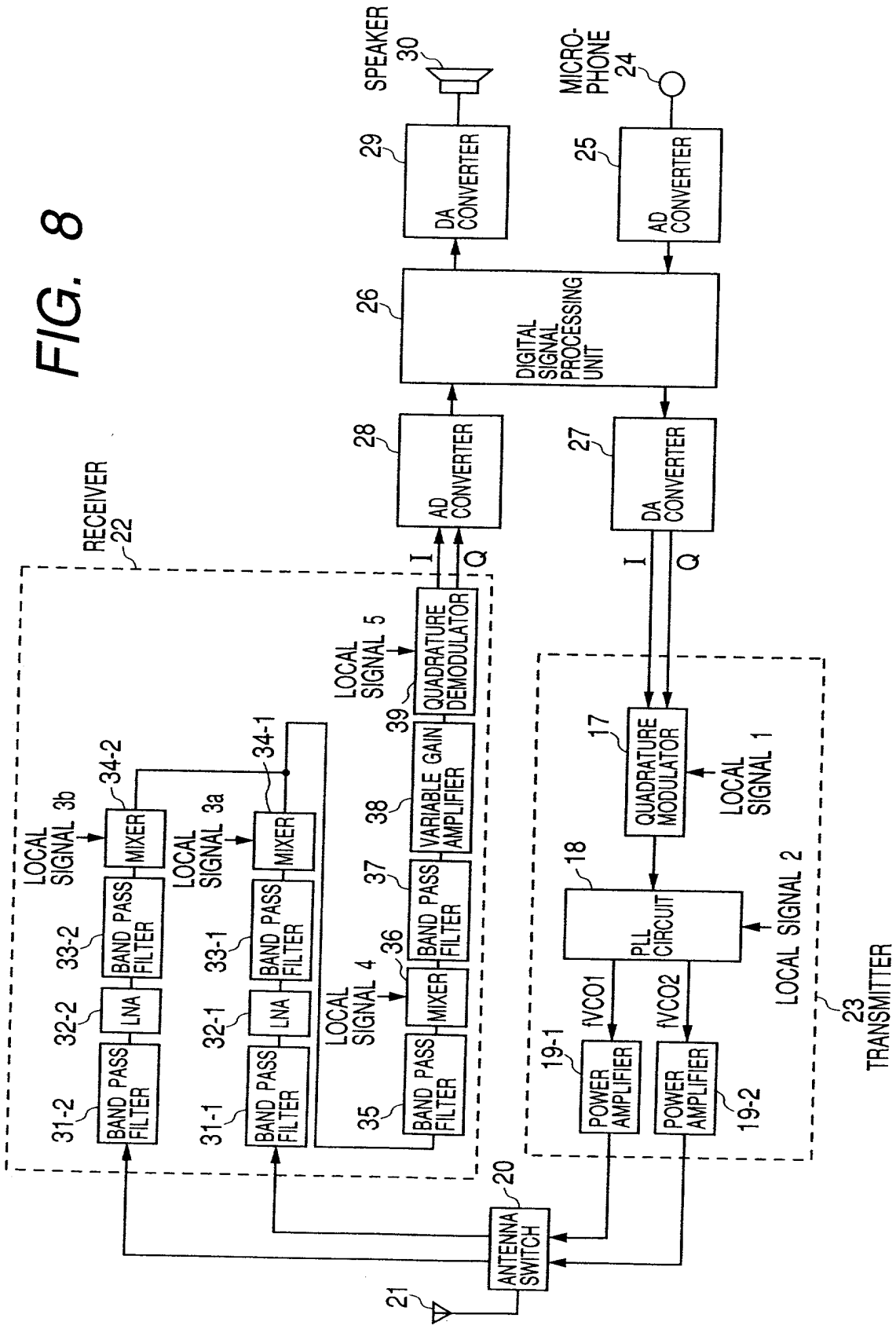
QUADRATURE MODULATOR
I
Q
IF
RF-LO
23
TRANSMITTER

FIG. 8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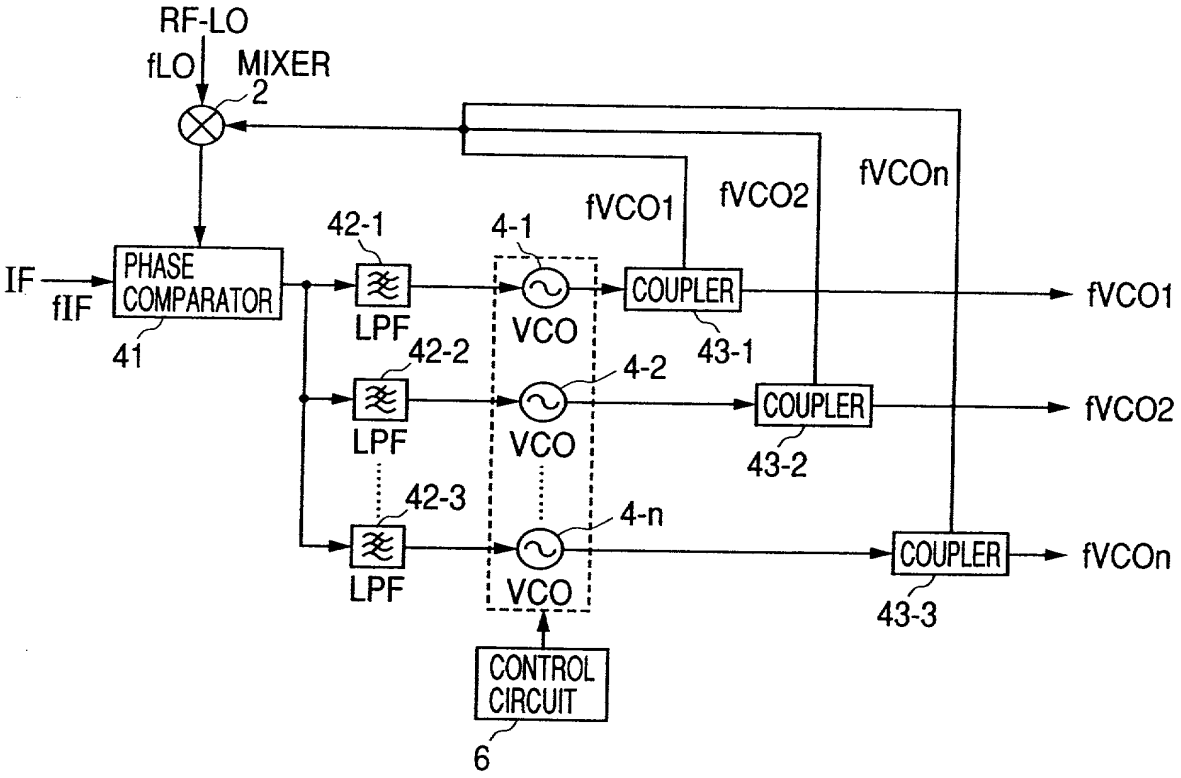
MICRO-PHONE
24
29
DA CONVERTER
25
AD CONVERTER
26
DIGITAL SIGNAL PROCESSING UNIT
28
AD CONVERTER
27
DA CONVERTER
RECEIVER
22
I
Q
I
Q
LOCAL SIGNAL 5
39
QUADRATURE DEMODULATOR
17
QUADRATURE MODULATOR
LOCAL SIGNAL 1
LOCAL SIGNAL 3b
34-2
MIXER
LOCAL SIGNAL 3a
34-1
MIXER
38
VARIABLE GAIN AMPLIFIER
18
PLL CIRCUIT
LOCAL SIGNAL 2
33-2
BAND PASS FILTER
33-1
BAND PASS FILTER
37
BAND PASS FILTER
32-2
LNA
32-1
LNA
LOCAL SIGNAL 4
36
MIXER
fVCO1
fVCO2
19-1
POWER AMPLIFIER
19-2
POWER AMPLIFIER
31-2
BAND PASS FILTER
31-1
BAND PASS FILTER
35
BAND PASS FILTER
LOCAL SIGNAL
23
TRANSMITTER
20
ANTENNA SWITCH
21

FIG. 9


RF-LO
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MIXER
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IF
fIF
PHASE COMPARATOR
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42-1
LPF
4-1
VCO
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fVCOn
COUPLER
43-1
fVCO1
42-2
LPF
4-2
VCO
COUPLER
43-2
fVCO2
42-3
LPF
4-n
VCO
COUPLER
43-3
fVCOn
CONTROL CIRCUIT
6

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Attorney Docket Number	843.39887X00

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I am the :

☐ Applicant.

☐ Assignee of record of the entire interest.
Certificate under 37 CFR 3.73(b) is enclosed.

[X] Attorney or agent of record .

Typed or Printed Name	Gregory E. Montone Registration NO. 28,141
Signature	
Date	March 19, 2001

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Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PLL CIRCUIT AND RADIO COMMUNICATION TERMINAL APPARATUS USING THE SAME

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
(該当する場合) _____に訂正されました。

☒ was filed on September 14, 1999
as United States Application Number or
PCT International Application Number
PCT/JP99/05012 and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

PTO/SB/106(8-96)
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Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条 (a) - (d) 項又は３６５条 (b) 項に基き下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約３６５ (a) 項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示している。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
10-262561	Japan	17/September/1998	☐
			☐

私は、第３５編米国法典１１９条 (e) 項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条 (c) に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Patent and Trademark Office; U.S. DEPARTMETNT OF COMMERCE

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

Donald R. Antonelli, Reg. No. 20,296; David T. Terry, Reg. No. 20,178; Melvin Kraus, Reg. No. 22,466; William I. Solomon, Reg. No. 28,565; Gregory E. Montone, Reg. No. 28,141; Ronald J. Shore, Reg. No. 28,577; Donald E. Stout, Reg. No. 26,422; Alan E. Schiavelli, Reg. No. 32,087; James N. Dresser, Reg. No. 22,973 and Carl I. Brundidge, Reg. No. 29,621

10

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Direct Telephone Calls to: (*name and telephone number*)

Telephone: (703) 312-6600
Fax: (703) 312-6666

唯一または第一発明者	1-10 Full name of sole or first inventor YAMAWAKI, Taizo
発明者の署名　　日付	Inventor's signature　　Date Taizo Yamawaki　　5/25/2001
住所	Residence Tokyo, Japan　JP
国籍	Citizenship Japan
私書箱	Post Office Address c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan

(第二以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for second and subsequent joint inventors.)

第二共同発明者		Full name of second joint inventor, if any ENDO, Takefumi
第二共同発明者の署名	日付	Second inventor's signature Date Takefumi Endo 5/30/2001
住所		Residence Takasaki, Japan JPY
国籍		Citizenship Japan
私書箱		Post Office Address C/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan
第三共同発明者		Full name of third joint inventor, if any WATANABE, Kazuo
第三共同発明者の署名	日付	Third inventor's signature Date Kazuo Watanabe 5/30/2001
住所		Residence ~~Takasaki,~~ Japan JPY
国籍		Citizenship Japan
私書箱		Post Office Address C/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan
第四共同発明者		Full name of fourth joint inventor, if any HORI, Kazuaki
第四共同発明者の署名	日付	Fourth inventor's signature Date Kazuaki Hori 5/31/2001
住所		Residence Yokohama, Japan JPY
国籍		Citizenship Japan
私書箱		Post Office Address C/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan
第五共同発明者		Full name of fifth joint inventor, if any HILDERSLEY, Julian
第五共同発明者の署名	日付	Fifth inventor's signature Date
住所		Residence
国籍		Citizenship United Kingdom
私書箱		Post Office Address C/o TTPCom Limited Melbourn Science Park, Cambridge Road Melbourn, Royston Hertfordshire, SG8 6EE, UNITED KINGDOM GBX

(第六以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for sixth and subsequent joint inventors.)

PTO/SB/106(8-96)
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Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

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PLL CIRCUIT AND RADIO COMMUNICATION TERMINAL APPARATUS USING THE SAME

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
(該当する場合) _____に訂正されました。

☒ was filed on September 14, 1999
as United States Application Number or
PCT International Application Number
PCT/JP99/05012 and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
10-262561	Japan	17/September/1998	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
			☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	

私は、第３５編米国法典１１９条 (e) 項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Patent and Trademark Office; U.S. DEPARTMETNT OF COMMERCE
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Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

10 Donald R. Antonelli, Reg. No. 20,296; David T. Terry, Reg. No. 20,178; Melvin Kraus, Reg. No. 22,466; William I. Solomon, Reg. No. 28,565; Gregory E. Montone, Reg. No. 28,141; Ronald J. Shore, Reg. No. 28,577; Donald E. Stout, Reg. No. 26,422; Alan E. Schiavelli, Reg. No. 32,087; James N. Dresser, Reg. No. 22,973 and Carl I. Brundidge, Reg. No. 29,621

書類送付先

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1300 North Seventeenth Street
Arlington, Virginia 22209

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Direct Telephone Calls to: (*name and telephone number*)

Telephone: (703) 312-6600
Fax: (703) 312-6666

唯一または第一発明者	Full name of sole or first inventor YAMAWAKI, Taizo
発明者の署名 日付	Inventor's signature Date
住所	Residence Tokyo, Japan
国籍	Citizenship Japan
私書箱	Post Office Address c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan

(第二以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for second and subsequent joint inventors.)

第二共同発明者	Full name of second joint inventor, if any ENDO, Takefumi
第二共同発明者の署名　日付	Second inventor's signature　Date
住所	Residence Takasaki, Japan
国籍	Citizenship Japan
私書箱	Post Office Address C/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan
第三共同発明者	Full name of third joint inventor, if any WATANABE, Kazuo
第三共同発明者の署名　日付	Third inventor's signature　Date
住所	Residence Takasaki, Japan
国籍	Citizenship Japan
私書箱	Post Office Address C/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan
第四共同発明者	Full name of fourth joint inventor, if any HORI, Kazuaki
第四共同発明者の署名　日付	Fourth inventor's signature　Date
住所	Residence Yokohama, Japan
国籍	Citizenship Japan
私書箱	Post Office Address C/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan
第五共同発明者	Full name of fifth joint inventor, if any HILDERSLEY, Julian
第五共同発明者の署名　日付	Fifth inventor's signature　Date Julian Hildersley. 11th June 2001
住所	Residence 21, LOTFIELD St., ORWELL, ROYSTON HERTS, SG8 5QT, ENGLAND.
国籍	Citizenship United Kingdom
私書箱	Post Office Address C/o TTPCom Limited Melbourn Science Park, Cambridge Road Melbourn, Royston Hertfordshire, SG8 6EE, UNITED KINGDOM

(第六以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for sixth and subsequent joint inventors.)